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InGaAs MISFETs with 0.7 μm gate lengths and 0.2 mm gate widths have demonstrated an output power density of 0.92 W/mm at 18 GHz with a corresponding power gain and power-added efficiency of 3.2 dB and 29%, respectively. At 20 GHz, an output power density of 0.79 W/mm was obtained with a corresponding gain and power-added efficiency of 3.0 dB and 23%, respectively.

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InGaAs/InP Submicron Gate Microwave Power Transistors For 20 GHz Applications

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ABSTRACT

InGaAs MISFETs with 0.7 um gate lengths and 0.2 mm gate widths have demonstrated an output power density of 0.92 W/mm at 18 GHz with a corresponding power gain and power-added efficiency of 3.2 dB and 29%, respectively. At 20 GHz, an output power density of 0.79 W/mm was obtained with a corresponding gain and power-added efficiency of 3.0 dB and 23%, respectively.

1. INTRODUCTION

Indium gallium arsenide (InGaAs) is a promising electronic material for high frequency applications. $In_{0.53}Ga_{0.47}As$ lattice matched to semi-insulating (SI) InP has higher low field mobility, peak electron velocity, and intervalley separation than InP [1]. Thus, InGaAs MISFETs have potential for superior microwave performance compared to InP MISFETs. InGaAs MISFETs with 1 um gate lengths have recently demonstrated output power densities greater than 1 W/mm of gate width at 9.7 GHz [2]. However, there have been very few reports on the output power performance of InGaAs MISFETs at K-band [3]. This paper reports on the fabrication of submicron gate length InGaAs MISFETs using an epitaxial process. The dc characteristics and rf power performance at 18 GHz and 20 GHz are presented.

2. EXPERIMENTAL

The depletion mode InGaAs MISFETs were fabricated on layers grown lattice matched on semi-insulating (SI) InP substrates using metal-

organic chemical vapor deposition (MOCVD). An InP buffer layer was grown unintentionally doped to a thickness of 0.2 um. The thickness of the InGaAs active layer ($n = 2 - 3 \times 10^{17}$ cm^{-3}) was 0.3 um. The layers were deposited using a horizontal, low pressure (2000 Pa) reactor. The In and Ga sources were trimethylindium (TMIn) and trimethylgallium (TMGa). The As and P sources were arsine (AsH_3) and phosphine (PH_3). The active layer doping was achieved using a diluted SiH_4 source. The growth temperature was 600 C. The growth rates for the InGaAs and InP layers were 2.9 um/hr and 1.3 um/hr, respectively. The lattice parameter was $< \pm 5 \times 10^{-4}$. The InGaAs mobility at 300 K was 5500 cm^2/V sec.

For the device fabrication, the samples were initially cleaned using standard solvents, a DI water rinse, an $HF:H_2O$ solution, and a final DI water rinse. After the initial clean, a mesa etch was performed for device isolation using a $H_2SO_4:H_2O_2:H_2O$ solution. Source/drain contacts (Au:Ge/Au) were then evaporated and defined using a liftoff process. The channel region was chemically recessed using a $H_2SO_4:H_2O_2:H_2O$ solution.

A silicon oxide gate insulator was then plasma deposited to a thickness of 500 Å [4]. The films were deposited using a Technics PlanarEtch IIA plasma system modified for 13.56 MHz operation. The silicon dioxide films were deposited at a pressure of 350 mTorr using 50 W of rf power, a SiH_4 flow rate of 19 sccm, a N_2O flow rate of 55 sccm, and a substrate temperature of 250 C. The gate insulators were subsequently annealed at 300 C in hydrogen.

The gate metallization (Ti/Au) was then evaporated and defined using a liftoff technique. Finally, source/drain oxide windows were opened and a Au overlayer was evaporated and defined by liftoff.

3. RESULTS

The completed InGaAs MISFETs had a source/drain contact spacing of 5 um. The length of the gate recess was 1 um and the gate length was 0.7 um. The devices had typical source-drain breakdown voltages of 6 - 8 V. The gate-source and gate-drain breakdown voltages were typically greater than 20 V. The device transconductance was typically 70 mS/mm of gate width.

The output power and power-added efficiency as a function of input power (11 - 20 dBm) for a 0.7 um gate length InGaAs MISFET with a total gate width of 0.2 mm is shown in Figure 1. The measurements were performed at a frequency of 18 GHz using a drain-source bias of 6.8 V and a gate-source bias of -1.8 V. The device saturation current density was about 500 mA/mm of gate width. The linear gain was about 6.2 dB. An output power density of 0.92 W/mm of gate width was obtained with a corresponding power gain and power-added efficiency of 3.2 dB and 29%, respectively, at an input power of 19.5 dBm. The highest power-added efficiency obtained was 32% with a corresponding power gain and output power density of 4.3 dB and 0.86 W/mm, respectively.

Figure 2 shows the output power performance at 20 GHz. The drain-source bias and gate-source bias were 7.0 V and -3.0 V, respectively. The linear gain was about 5.1 dB. An output power density of 0.79 W/mm was obtained with a corresponding power gain and power-added efficiency of 3.0 dB and 23%, respectively, at an

input power of 19 dBm. The highest power-added efficiency obtained was 25% with a corresponding output power density and gain of 0.73 W/mm and 3.7 dB, respectively.

4. SUMMARY

Depletion mode InGaAs MISFETs with submicron gate lengths were fabricated using an epitaxial process. A plasma deposited silicon dioxide gate insulator was used as the gate insulator. At 18 GHz, an output power density of 0.92 W/mm was obtained at an input power of 19.5 dBm. The corresponding gain and power-added efficiency were 3.2 dB and 29%, respectively. The highest power-added efficiency obtained was 32% with a corresponding power gain and output power density of 4.3 dB and 0.86 W/mm, respectively, at an input power of 18 dBm. At 20 GHz, an output power density of 0.79 W/mm was obtained with a corresponding gain and power-added efficiency of 3.0 dB and 23%, respectively. The highest power-added efficiency was 25% at 0.73 W/mm output power density and 4.8 dB gain.

5. ACKNOWLEDGEMENTS

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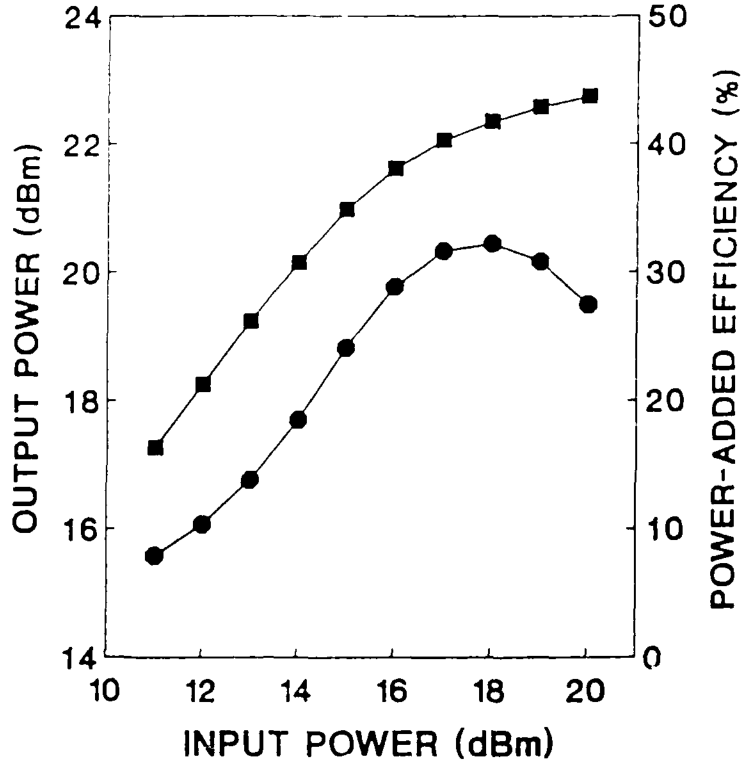

Figure 1

Output power, power-added-efficiency vs. input power (18 GHz)

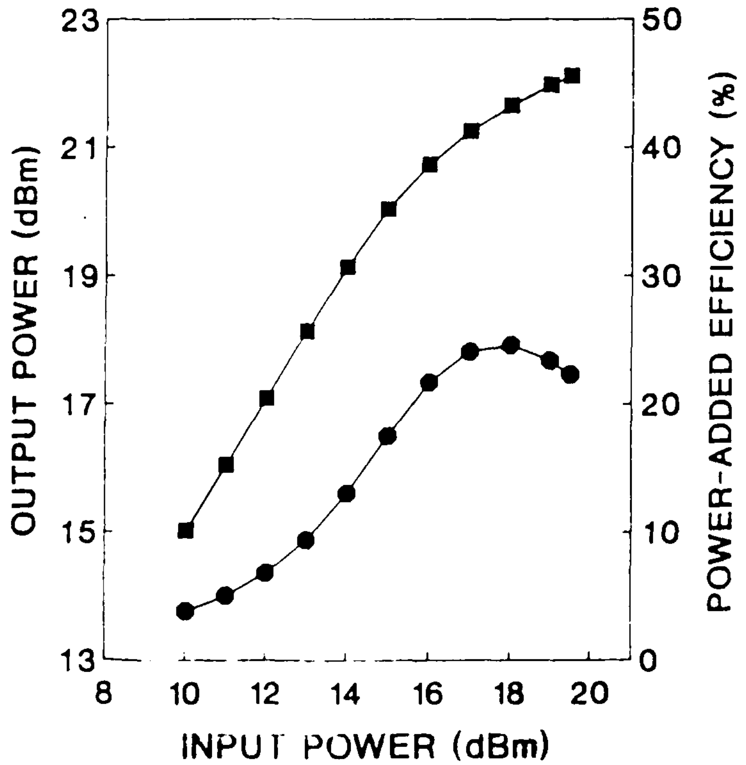

Figure 2

Output power, power-added-efficiency vs. input power (20 GHz)